Controller Command Description

This document describes the commands executed by a controller that contains a 250 Mhz timing board (ARC-22) and a utility board (ARC-30) that is written to operate CCD arrays. Most, but not all, of the commands are implemented in systems for operating IR arrays, so the user should consult the command table near the end of the file named "tim.asm" to see what is implemented. In this document there is a set of common terms and definitions:

- “"Controller"” below refers to either the timing or the utility board, meaning that the command may be directed to and executed by either the timing or the utility board. "Timing" means the command may only be executed by the timing board.
- All successful commands reply with an ASCII done (‘DON’), unless specified otherwise. Unsuccessfully executed commands may return an ASCII error (‘ERR’) or timeout (‘TOUT’).
- The PCI device driver expects that all unused command arguments be set to -1.
- The command header is specified as follows:

  Header = 0x00ddnn
  Where dd = destination bye = 2 for timing board and 3 for utility board.
  Where nn = number of words in command (including header) = (1 (header) + 1 (command) + number of arguments) >= 2.

  The first byte of the command header is the source number, which is 00 for all the commands described herein. There are some commands, not described here, that the timing board originates that are directed to the utility or PCI boards, in which case the source byte is a 02. Reply headers are either 02 or 03 for the source byte and a 00 for the destination byte. In the text below a header of 0x0002nn indicates that the command is executable by the timing board only, and a header of 0x000ddnn is executable by either the utility or the timing board.

I. BOOT COMMANDS

These commands are resident in the controller board EEPROM and are loaded into the DSP memory whenever the power to the controller is turned on. These commands are listed at the end of the "timboot.asm" file.

TDL – Test Data Link

This command tests the communication link between the PCI interface board and the controller. The controller will return the command argument in its reply if the command executes properly.

Usage: 0x00dd03 <‘TDL’> <arg1>

- arg1 may be any 24-bit number
- Reply is arg1 if the command succeeded

RDM – Read Memory

This allows the host computer to read any controller DSP or EEPROM memory location. The command replies with the 24-bit value stored at the specified memory location.

Usage: 0x00dd03 <'RDM'> <arg1>

- arg1 is <type | memory address> where type may be one of the following DSP memory types:
  P (0x100000) DSP Program memory
  X (0x200000) DSP X memory
  Y (0x400000) DSP Y memory
  R (0x800000) EEPROM memory
- Reply is the value stored at the memory address.

WRM – Write Memory

This allows the host computer to write to any DSP or EEPROM memory location.

Usage: 0x00dd04 <'WRM'> <arg1> <arg2>

- arg1 is <type | memory address> where type may be one of the following DSP memory types:
  P (0x100000) Program
  X (0x200000) X space
  Y (0x400000) Y space
  R (0x800000) Rom space
- arg2 may be any 24-bit number

LDA – Load Application

This instructs the controller to load an application from EEPROM to DSP memory.

Usage: 0x00dd03 <'LDA'> <arg1>

- arg1 may be any valid application number, which is from 0 to 3.

STP – Stop Idle Clocking

The timing board continuously clocks the CCD if it is in 'idle' mode when it is not reading out, exposing or executing other commands. The STP command instructs the timing board to exit the 'idle' mode and not clock out the CCD.

Usage: 0x000202 <'STP'>

II. APPLICATION COMMANDS

These are commands that can be executed only after application code is downloaded from the host computer to the controller or loaded from on-board EEPROM into the DSP memory with the LDA command. These commands are listed towards the end of the "tim.asm" file.

PON – Power On

This instructs the controller to turn on the analog voltages to the controller backplane by closing the switches located on the power control board.

Usage: 0x00dd02 <'PON'>

POF – Power Off

This instructs the controller to turn off the analog voltages to the controller backplane by opening the switches located on the power control board.

Usage: 0x00dd02 <'POF'>

SBV – Set Bias Voltage

This instructs the timing board to read all the entries in the "DAC" waveform table and write them to the DACs in the controller.

Usage: 0x000202 <'SBV'>

IDL – Start Idle Clocking

The timing board continuously clocks the CCD if it is in 'idle' mode when it is not reading out, exposing or executing other commands. IDL commands the timing board to clock the CCD under these circumstances.

Usage: 0x000202 <'IDL'>

OSH – Open Shutter

This instructs the controller to open the shutter. The timing board generates a TTL signal that is routed to the small power supply to a shutter driver circuit that generates a high voltage pulse useful for opening solenoid operated shutters. The utility board controls an open collector signal pulled up to +5 volts. All three of these signals (TTL, solenoid pulse and open collector) are wired to the shutter connector on the back of the controller housing. The TTL and open collector signals are low to open the shutter.

Usage: 0x00dd02 <'OSH'>

CSH – Close Shutter

This instructs the controller to close the shutter. See OSH for more info.

Usage: 0x00dd02 <'CSH'>

RDC – Read CCD

This instructs the timing board to begin reading out the CCD and transmitting pixel data to the PCI board.

Usage: 0x000202 <‘RDC’>

CLR – Clear Array

This instructs the timing board to perform a fast clear of the CCD.

Usage: 0x000202 <‘CLR’>

SET – Set Exposure Time

This sets the exposure time in milliseconds in the timing board. This is used by the 'SEX' command, described below, to set the time between the end of clearing the CCD and the beginning of readout. The utility board may also be used to control exposures, in which case the exposure time is set by writing to the memory location Y:0x18 with the WRM command.

Usage: 0x000203 <‘SET’> <arg1>

- arg1 is the exposure time in milliseconds

RET – Read Elapsed Exposure Time

This returns the elapsed exposure time in milliseconds from the timing board. The elapsed time increments from zero to 'exposure time'. If the utility board is used then the elapsed exposure time may be read from Y:0x18.

Usage: 0x000202 <‘RET’>

- Reply is the elapsed exposure time in milliseconds

SEX – Start Exposure

This instructs the controller to start an exposure, which involves clearing the array, operating the shutter, starting the exposure timer, waiting until the exposure timer reaches the exposure time and initiating readout. It may be issued to either the timing or utility board.

Usage: 0x00dd02 <‘SEX’>

PEX – Pause Exposure

This instructs the controller to pause an exposure, which causes the shutter to close and the exposure timer to stop. The CCD will not be clocked.

Usage: 0x00dd02 <‘PEX’>

REX – Resume Exposure

This instructs the controller to resume a paused exposure. The shutter is re-opened (if needed) and the exposure timer is re-started from where it left off.

Usage: 0x00dd02 <‘REX’>

AEX – Abort Exposure

This instructs the controller to abort an exposure. The shutter is closed, the exposure timer is stopped, and the controller resumes idle mode (where the array is continuously clocked). No image data is transferred.

Usage: 0x00dd02 <'AEX'>

ABR – Abort Readout

This instructs the timing board to immediately stop the CCD readout.

Usage: 0x000202 <'ABR'>

CRD – Continue Readout

This instructs the timing board to continue readout of the array if any command was issued during the readout. Commands should not normally be sent to the controller during readout because execution of the command will interrupt the readout, and the readout can only be resumed by issuing this command.

Usage: 0x000202 <'CRD'>

SGN – Set Gain

This instructs the timing board to set the video processor gain and integrator speed for all video boards. A fast gain control setting selects a 1 nanofarad capacitor to be used in the dual-slope integrator and provides a much larger gain than the slow setting which selects a 4.9 nanofarad capacitor. This instruction is sent to the timing board only.

Usage: 0x000204 <'SGN'> <arg1> <arg2>

- arg1 is the video processor gain and may be 1, 2, 5, or 10.
- arg2 is the integrator speed and may be 0 for fast or 1 for slow.

SBN – Set Bias Number

This writes a number to a selected DAC for setting its output voltage. These DACs are used for generating DC bias voltages, clock driver voltages, and video offsets.

Usage: 0x000206 <'SBN'> <arg1> <arg2> <arg3> <arg4>

- arg1 is the board number (0 – 15)
- arg2 is the DAC number
- arg3 is ''VID'' or ''CLK'' for video processor and clock driver, respectively
- arg4 is a 12-bit number (0 to 4095) that sets the voltage

SMX – Set MUX

This sets the MUX value to be output on the clock driver board. This instruction is sent to the timing board only.

Usage: 0x000205 <'SMX'> <arg1> <arg2> <arg3>

- arg1 is the board number (0 to 15)

- arg2 is the MUX1 value (0 to 23)
- arg3 is the MUX2 value (0 to 23)

CSW – Clear Switches

This clears all the analog switches in the system, useful for keeping the switch power dissipation to a minimum prior to powering on the analog supplies. This instruction is executed by the timing board only.

Usage: 0x000202 <'CSW'>

SOS – Select Output Source

This selects which amplifier(s) will be used for readout. This instruction is executed by the timing board only.

Usage: 0x000203 <'SOS'> <arg1>

- arg1 is the amplifier name. It may be one of the following:

Both Single and Parallel readout

__A (0x5F5F41) Upper Left Amp
__B (0x5F5F42) Upper Right Amp
__C (0x5F5F43) Lower Left Amp
__D (0x5F5F44) Lower Right Amp
_AB (0x5F4142) Upper Two Amps
_CD (0x5F4344) Lower Two Amps
ALL (0x414C4C) Quad Readout

Serial readout only

__L (0x5F5F4C) Lower Left Amp
__R (0x5F5F52) Lower Right Amp
_LR (0x5F4C52) Split Serial Readout

SSS – Set Subarray Size

This instructs the timing board to set the subarray image parameters, which are subarray width, height and bias width. The bias region's height is taken to be the same as the subarray box. The details of this command are further described in the voodoo users manual.

Usage: 0x000205 <'SSS'> <arg1> <arg2> <arg3>

- arg1 is the bias region width (in pixels)
- arg2 is the subarray width (in pixels)
- arg3 is the subarray height (in pixels)

SSP – Set Subarray Position

This instructs the timing board to set the subarray image positions, which are subarray and bias region coordinates. The details of this command are further described in the voodoo users manual.

Usage: 0x000205 <'SSP'> <arg1> <arg2> <arg3>

- arg1 is the subarray Y position. This is the number of rows (in pixels) to the lower left corner of the desired subarray region.
- arg2 is the subarray X position. This is the number of columns (in pixels) to the lower left corner of the desired subarray region.
- arg3 is the bias region offset. This is the number of columns (in pixels) to the left edge of the desired bias region.

RCC – Read Controller Configuration

This instructs the timing board to return the 24-bit controller configuration word. The bits of this word determine what hardware and software capabilities are implemented in the system. The bits are all defined in the file named 'timhdr.asm'.

Usage: 0x000202 <'RCC'>

- Reply is the 24-bit controller configuration word

III. OPTIONAL APPLICATION COMMANDS

The following commands are not implemented on all controllers. Users should consult the command list towards the end of the "tim.asm" file.

SDM – Set Dither Mode

This instructs the timing board to exercise the parallel clocks during readout as a way of reducing the dark current.

Usage: 0x000202 <'SDM'>

SSM – Set Sync Mode

This instructs the timing board to set up for synchronized image readout. Generally, exposure start will only begin when an external SYNC pulse to the timing board is asserted high (true). In the meantime the CCD is continuously parallel clocked, with the serial registers held high.

Usage: 0x000202 <'SSM'>

SPT – Set Pixel Time

The argument will be the number of 40 nanosec clock ticks assigned for integrating the reset level of the CCD output, followed by the same time devoted to integrating the CCD signal after the summing well charge has been dumped onto the output node.

Usage: 0x000203 <'SPT'> < arg1 >

- arg1 is the number of 40 ns clock ticks

SNC – Set Number of Coadds

The argument will be the number frames that will be generated each time the SEX command is issued. Setting a value greater than 1 places the controller in

continuous readout mode wherein it generates the requested number of frames without further command and instructs the PCI board when to restart its PCI image address at the base address. The host computer may either coadd these frames together into one composite 32-bit per pixel image or store them individually on disk.

Usage: 0x000203 < SNC > < arg1 >>

- arg1 is the number of image frames

FPB – Set Number of Frames per Buffer

The argument will be the number CCD frames that will be written to one image buffer of the host computer. After this number of frames have been transferred to the PCI board in continuous readout mode, the timing board will send an 'IIA' command to the PCI board, instructing it to write the next 'arg1' frames starting at the base PCI image address. The host computer application must transfer the image data out of the image frame buffer to avoid data loss, as this implements a circular image buffer. Generally the host computes the number of frames per buffer from the frame size and the allocated image buffer size.

Usage: 0x000203 < FPB > < arg1 >

- arg1 is the number of frames that can be stored in the current host computer image buffer.

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