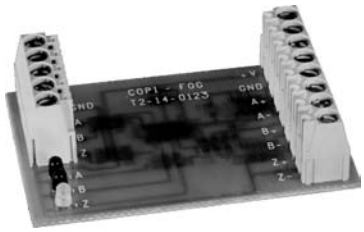
Support Equipment

CP-1000, Optoboard



Description:

The CP-1000 is a convenient and cost-effective way to convert single ended encoder signals into differential line driver signals. The input signals are optically isolated from the output signals. The PCB is dimensioned to fit standard DIN rails for easy mounting.

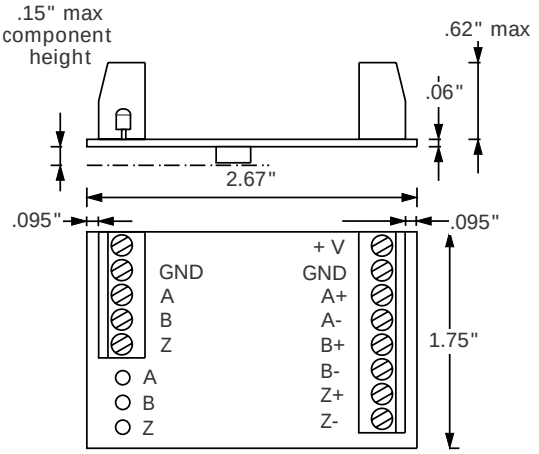
Specifications:

power in:	+5 Vdc - 15 Vdc @ 20 mA max (no load)
input signals:	single ended 5 to 15 volt
max. frequency:	500 KHz (A or B ch.)
output signals:	differential linedriver (88C30)

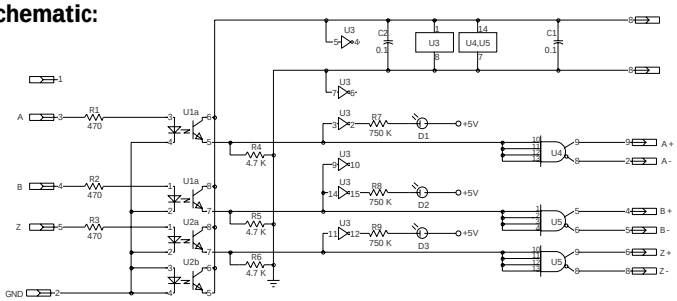
Ordering Information:

CP-1000. For different encoder signal levels, please contact the factory.

Mechanical:



Schematic:



CP-1001, Encoder Interface Unit

Description:

The CP-1001 is a convenient and cost-effective way to convert single ended encoder signals into differential line driver signals. LED's indicate status of all input and output signals thus aiding system diagnosis.

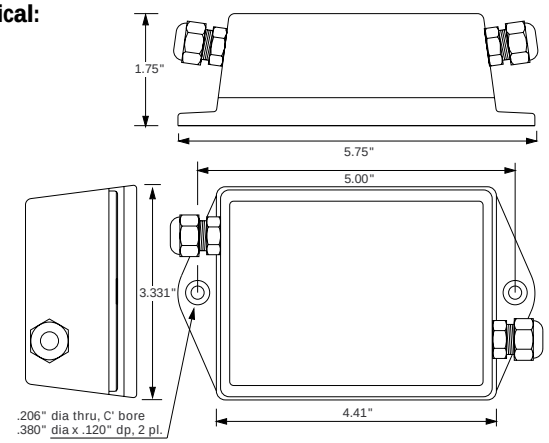
Specifications:

power in:	+5 to +24 Vdc
input signals:	single ended 5 to 24 volt
max. frequency:	500 KHz (A or B ch.)
output signals:	differential linedriver (ET7272)

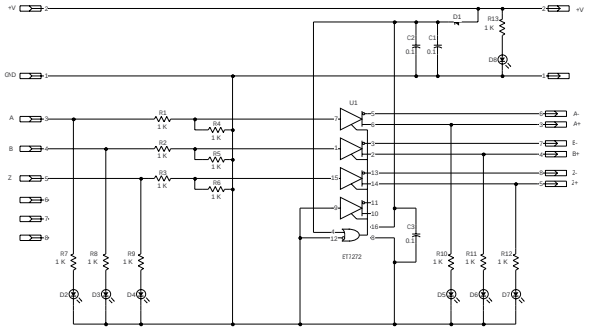
Ordering Information:

CP-1001.

Mechanical:



Schematic:



CP-1002, Universal Counter

Description:

The CP-1002 is a Universal Counter that can be set up to count up/down, quadrature, anti-coincidence counting, and more. Operating modes are DIP switch selectable including the decimal point on the display. Inputs are optically isolated to provide trouble free operation.

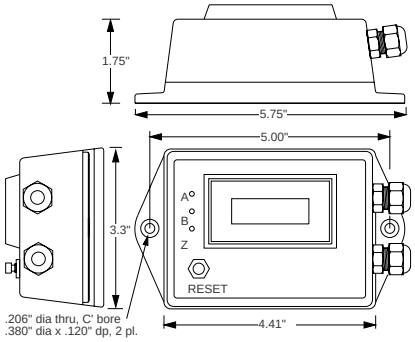
Internal scaling of 1X, 2X, 4X, divide-by-2.5, divide-by-5, divide-by-10, divide-by-25, divide-by-50, and divide-by-100.

Specifications:

power in:	5 Vdc ± 10% @ 50 mA
input signals:	single ended or differential
max. frequency:	200 KHz (A or B ch.)

Ordering Information:

CP-1002-TTL.



CP-1003, HHC Counter

Description:

The CP-1003 is similar to the CP-1002 Universal Counter except it has our proprietary 64X Interpolator (CP-1064) and a divide-by-n circuitry. This provides unparalleled value for measuring systems in that an inexpensive sine/cosine encoder (i.e. CP-200/300/500/800) can be used to give any resolution up to 1,440,000 measuring steps.

Specifications:

power in:	5V
input signals:	sine/cosine, 1V p-p
max. frequency:	100 KHz
output signals:	complementary linedrivers, RS 422 compatible.

Ordering Information:

CP-1003-(1)

(1): 64 = 64x ; 32 = 32x ; 16 = 16x

CP-1004, Qdapter

Description:

The CP-1004 quadrature adapter (Qdapter) provides a unique way of matching almost any encoder to any application. Internal high efficiency switching voltage regulators allows electrical interface compatibility between encoder and controller while special scaling circuitry provides resolution matching. Available with optional display counter.

Ordering Information:

CP-1004-1
(1): N = no counter ; C = with display counter

Resolution Conversion:
any encoder resolution may be converted to any other lower resolution (i.e. encoder with 2048 cycles may be converted to 1800 cycles of quadrature) and is programmable using any PC with a serial port.

May be powered from 5 to 30 volts and will power encoders requiring the same or lower supply voltages. Input quadrature/index signals may be single-ended or differential signals and opto-isolation is provided. Mechanically per the CP-1002/1003

CP-1005/1006, Absolute/Fiberoptic to Quadrature Interfaces

CP-1005 Absolute to Quadrature Interface

Description:

Using absolute encoders greatly enhances system reliability and the CP-1005 provides a convenient way to interface absolute encoders to the more common quadrature interface ports on logic and motion controllers.

Ordering Information:

CP-1005-(1)

(1): S = serial input
(use w/ CP-850/950-24MT)
P = parallel input
(use w/ CP-850-12GC)

CP-1006 Fiberoptic to Quadrature Interface

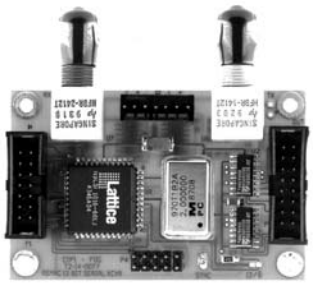
Description:

The CP-1006 is similar to our CP-1112 (see CP-1012 or CP-860 datasheets) except that this unit comes with terminal blocks and water tight strain reliefs for round cables. The unit will convert fiberoptic signals from our Fiberoptic Link compatible products to electrical signals. Also available with optional counter display.

Ordering Information:

CP-1006-(1)

(1): N = no counter
C = w/ display counter



Description:

The CP-1012 is an asynchronous transceiver which will transmit 12 independent signals over a single fiberoptic cable or a single twisted pair without the need for a clock signal.The unit consists of completely separate receiver and transmitter sections which can be wired to allow "daisy chaining" of data from different locations.

In fiberoptic mode, the transmission is noise-free and immune to EMF, RFI, lightening strikes etc. Cables, cut to length and terminated are factory available.
The twisted-pair mode is a cost-effective solution in less noisy environments or for short connections if transmission speed is a concern.

Ordering Information:

fiberoptic link, transceiver
p/n CP-1012-20M-5-TR

fiberoptic link, receiver-only
p/n CP-1012-20M-5-R

twisted pair link, transceiver
p/n CP-1012-(clock speed)-5-LD. A clock speed of 2MHz is standard, 60 MHz highest available.

fiberoptic link, receiver-only in DB-25 connector
p/n CP-1112-20M-12-Rx (5 Vdc in/out only)
p/n CP-1112-20M-12-R (8 - 15 Vdc in/out only)

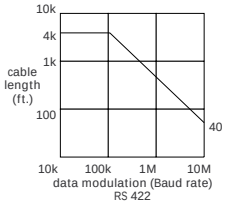
cable (factory terminated)]
p/n 2-02-0247- (cable length in feet)

terminator kit (for in-house termination of cable):
p/n 2-00-0098

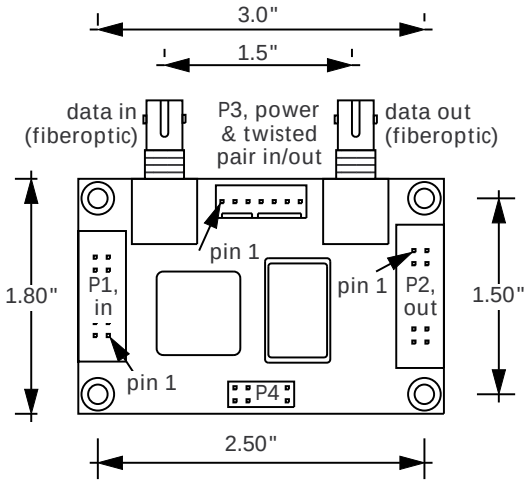
Specifications:

power input:	+ 5Vdc ± 5% @ 75 mA max., no external loads
output format, connector P2:	12 bit parallel, TTL compatible
input format, connector P1:	12 bit parallel, TTL compatible
twisted pair receiver:	differential line receiver 26LS32
twisted pair transmitter:	differential line driver MC3487, RS 422 & DIN 66259 part 3
update rate fiberoptic link:	compatible
update rate twisted pair link:	2.8 µs (20 MHz clock speed)
clock speed fiberoptic link:	0.93 µs @ 60 MHz clock speed
clock speed twisted pair link:	20 MHz (Baud rate of 5 MBaud) up to 60 MHz (Baud rate of up to 15 MBaud)
maximum distance fiberoptic link:	6000 feet
maximum distance twisted pair link:	speed dependent, see diagram

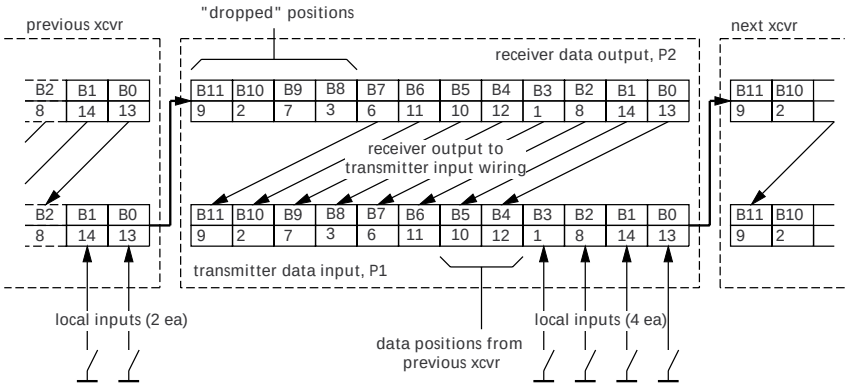
Recommended operating area for balanced differential line drivers and receivers (twisted pairs). Recommended terminating resistor value across Rx- and Rx+ : 100.



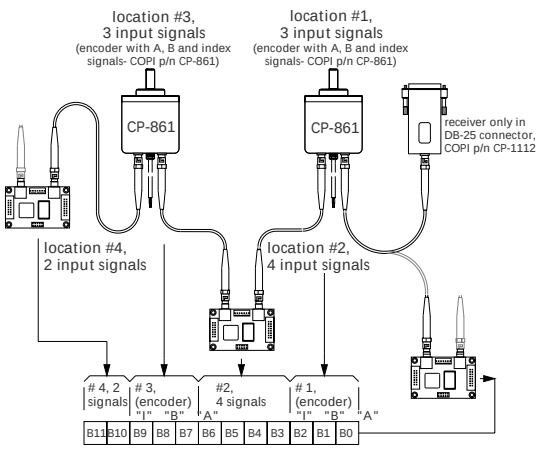
Mechanical:



"Daisy Chain" Receiver to Transmitter Wiring



"Daisy Chain" Example:



P1, transmitter input (14 pin header):

pin 1	B3
pin 2	B10
pin 3	B8
pin 4	B9
pin 5	ground
pin 6	B7
pin 7	+5Vdc
pin 8	B2
pin 9	B11
pin 10	B5
pin 11	B6
pin 12	B4
pin 13	B0
pin 14	B1

P2, receiver output (16 pin header):

pin 1	B3
pin 2	B10
pin 3	B8
pin 4	B9
pin 5	ground
pin 6	B7
pin 7	+5Vdc
pin 8	B2
pin 9	B11
pin 10	B5
pin 11	B6
pin 12	B4
pin 13	B0
pin 14	B1
pin 15	sync**
pin 16	strobe**

P3, power & twisted pairxcvrs (7 pin Molex):

pin 1	RX-*
pin 2	RX+*
pin 3	+5Vdc
pin 4	ground
pin 5	TX-*
pin 6	TX+*

* Rx- and Rx+ connect to Tx- and Tx+ resp. of a previous stage. Tx- and Tx+ connect to Rx- and Rx+ resp. of a next stage.

** Sync signal turns low when a reliable link has been established. The strobe signal indicates transfer of valid data to the reciever output register.

Description:

The CP-4016 interface board is a convenient way to connect four incremental encoders to an IBM-compatible PC. Included with the CP-4016 is a demo diskette with a simple program written in Quik Basic. The source listing is included along with an .EXE file. Reviewing the source listing should give adequate insight on how to access the data from the counters. The "TYPE" command will bring up the source listing. The CP-4016 can be installed in any slot, the default address is $3E0. The demo program is started by typing COP4V1_1 <cr> at the DOS prompt. The screen will then display a representation of the individual bits of each encoder's counter along with its numerical value. At the bottom of the screen is a display that corresponds to the function keys. F10 exits the program back to DOS. F6, F7, F8 and F9 toggles the source of the reset signal for each encoder. F1, F2, F3 and F4 will reset their respective counter if they are selected as source by F6, F7, F8 or F9.

Connection to the board from the encoders is made via a DB-25S connector (mating connector: DB-25P).

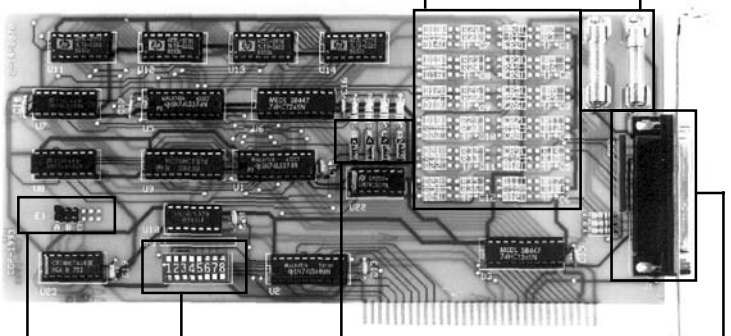
The board contains four HCTL 2016 quadrature decoder/16 bit up-down counter interfaces with integral digital filtering for noise immunity. The three main functions of the card are:

1) monitor the contents of each encoder position counter
2) select the source for each of the counter reset to zero signals
3) reset each of the counters, either by means of the corresponding encoder index signal or by means of a command from the host computer.

The above fuctions are accomplished by setting up the card with a few instructions, using the addressing and control formats below.

The card has two options that are controlled by jumper selection: E1 and E2. E1 sets the clock rate for the counters and also determines the filter action of the input circuit to the counter. E2 selects the true or inverse of the index to reset the position counter, the jumper in the top position will select the true signal, in the bottom position the inverse signal.

Utility software for use with the CP-4016 may be found on our website at the following address:
http://opticalencoder.com/utilities/cp-4016.html



DB 25 connector pinouts:

pin 1	encoder # 4, B channel *
pin 2	encoder # 4, A channel *
pin 6	encoder # 4, Index channel
pin 4	encoder # 3, B channel
pin 5	encoder # 3, A channel
pin 3	encoder # 3, Index channel
pin 7	encoder # 2, B channel
pin 8	encoder # 2, A channel
pin 12	encoder # 2, Index channel
pin 10	encoder # 1, B channel
pin 11	encoder # 1, A channel
pin 9	encoder # 1, Index channel
pin 13	no connection

pin 14, 17, 20, 23:	+ 12 Vdc out
pin 15, 18, 21, 24:	ground
pin 16, 19, 22, 25:	+ 5 Vdc out

* Increasing count is when channel A leads channel B (all encoders)

Addressing:

The 8 position DIP switch sets the top 8 address bits in the 0 - 3FF I/O space to select a block of 4 consecutive addresses:

address switch position:	1	2	3	4	5	6	7	8
0-3FF I/O space address lines:	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The "off" position of the address switches defines a "1" on the corresponding address line,so the following sequence defines "**3E0**" as the starting address of four I/O positions:

address switch position:	1	2	3	4	5	6	7	8
	off	off	off	off	off	on	on	on
0-3FF I/O space address lines:	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	3		E				0, 1, 2, & 3			

The definitions of these four positions is as follows:

3E0 selects the contents of a particular counter as well as the high byte/low byte for reading in the output register (control register "0")
3E1 selects reset modes (control register "1")
3E2 output of one counter out of four, high or low byte, as selected by the first control register (read register)
3E3 not defined

Control Register Format:

control register 0, read select:

	msb						lsb	
	8	7	6	5	4	3	2	1
	encoder 4:		encoder 3:		encoder 2:		encoder 1:	
read high byte:	0	0	0	0	0	0	0	0
read low byte	0	1	0	1	0	1	0	1

control register 1, position counter reset mode:

reset at index signal:

msb	8	encoder 4 index reset when set high (1)
	7	encoder 3 index reset when set high (1)
	6	encoder 2 index reset when set high (1)
	5	encoder 1 index reset when set high (1)

software reset:

	4	reset encoder 4 when set low (0)
	3	reset encoder 3 when set low (0)
	2	reset encoder 2 when set low (0)
lsb	1	reset encoder 1 when set low (0)

When using an external reset and while reading data if an encoder index signal occurs, latched data will change.